(10) ABSTRACT

Electrostatic discharge protection for integrated circuits, particularly for enhancing electrostatic discharge protection performance for Input-output cells and power supply clamps used in CMOS and BiCMOS IC technologies is described. A P-type, implantation region, or layer, referred to as "P-deep," in both N-MOSFET and P-MOSFET devices is provided to enhance electrostatic discharge protection performance. Parasitic transistor gain is enhanced by providing the P-deep region subposing the drain contact. Exemplary embodiments for N-type and P-type MOSFETs, MOSFETs with surface diodes, MOSFETS with SCRs, and push-pull Input-output CMOS circuits are described.